IN THE SPECIFICATION:

The newly-submitted Specification includes the new versions of the paragraphs having the following changes, which are detailed on separate pages below.

The paragraph found from page 8, line 17 through page 9, line 17 is replaced with the new version set forth on the attached page.

The paragraph found from page 17, line 12 through page 18, line 14 is replaced with the new version set forth on the attached page.

IN THE DRAWINGS:

The original Figure 5 is replaced with the accompanying new version of Figure 5.

The original Figures 8C through 8K are replaced with the accompanying new versions of Figures 8C through 8K.

IN THE CLAIMS:

Amend Claims 1 and 7 as set forth on the accompanying pages.

MARKED UP VERSION OF PARAGRAPH FROM P.8, L17-P.9,L17

In accordance with the present invention, a high dielectric constant material, which is process-compatible with the semiconductor chip processing, is provided between adjacent metal lines and/or adjacent metal layers on the chip itself. In yet another embodiment, the high dielectric constant material is provided between metal lines and/or between metal layers in a semiconductor packaging structure. The high dielectric constant material is chosen from the group consisting of ferroelectrics, relaxors, paraelectrics, perovskites, pyrochlores, layered perovskites or any material with a dielectric constant which is greater than or equal to 10. Examples of such materials include Ta_2O_5, $BaTiO_3$, $SrTiO_3$, $BaStTiO_3$ (BST or BSTO), $PbZrTiO_3$ (PZT), $PbZrO_3$, $PbLaTiO_3$ (PLT), and $SrBiTiO_3$ (SBT). In addition, any other dielectric material having a dielectric constant which is 2-3 times higher than that of conventional oxide, and which is process-compatible with the semiconductor chip processing (e.g., silicon nitride, aluminum oxide, TiO_2 HfO_2, etc.), can be used. Hereinafter, all eligible materials <u>will be</u> [with be] generically referred to as "high-k" materials.

NEW VERSION OF PARAGRAPH FROM P.8,L17-P.9,L17

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MARKED UP VERSION OF PARAGRAPH FROM P.17, L12-P.18, L14

To process further, a higher level of interconnect with a similar high-k material capacitor is formed. The process comprises first forming metal contact 815 with conductive adhesion liner 817 in second dielectric layer 812 as shown in Figure 8G. The metal contact [8159] 815 can be formed by Damascene processing such as is used to form metal wires. The second dielectric layer is patterned, for example by depositing a photoresist and etching an opening in the dielectric using a selective etch, as was described with reference to layer 802 above. Once the opening in the dielectric layer 812 has been defined, an electrically conductive diffusion material 827 is deposited on the top of the structure as shown in Fig. 8H. High-k material 819 is conformally deposited over the electrically conductive diffusion barrier layer 827 as shown in Fig. 8I. Thereafter, the high-k material is polished back to the electrically conductive diffusion barrier, as shown in Fig. 8J, followed by etching of the electrically conductive diffusion barrier layer 827. Another diffusion barrier metal 837 is deposited, followed by formation of a top metal wire 833 by metal etching

using a photoresist as a mask to first etch the metal and then remove the exposed diffusion barrier layer 837. The resulting cross-sectional view is shown in Fig. 8K. The high-k material 819 is sandwiched between two metal lines 805 and 833, thereby forming the vertical decoupling capacitor.

NEW VERSION OF PARAGRAPH FROM P.17, L12-P.18, L14

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